REMARKS/ARGUMENTS

The Applicants have carefully considered this Application in connection with the Examiner's Action and respectfully request reconsideration of this Application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-21 in the Application. The Applicants have amended Claims 1, 8 and 15 and have canceled Claims 5, 12 and 19 in a previous Amendment without prejudice or disclaimer. The Applicants also added dependent Claims 22 and 23 in a previous Amendment. Claims 22 and 23 are cancelled in the present Amendment without prejudice or disclaimer. Dependent Claims 24 -26 are added with this Amendment. Accordingly, Claims 1-4, 6-11, 13-18, 20-21, and 24-26 are currently pending in the Application.

Support for the present Amendments can be found at least on page 11, paragraph [0029] to page paragraph [0031], page 14 of the present Application.

I. Objections to Claims 22 and 23

The Examiner has objected to Claims 22 and 23 because of informalities. The Applicants have cancelled Claims 22 and 23without prejudice or disclaimer. The Applicants therefore request that the Examiner withdraw the objection.

II. Rejection of Claims 1-4, 6-11, 13-18 and 20-23 under 35 U.S.C. §103

The Examiner has rejected Claims 1-4, 6-11, 13-18 and 20-23 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,221,774 to Henry et al. ("Henry") in view of U.S. Patent No. 6,988,190 to Park ("Park"). The Applicants respectfully disagree.

As discussed in previous amendments, Henry relates to the prediction of conditional branch instruction outcomes associated with a microprocessor having a pipeline architecture. (*See* column 1, lines 8-10.) Henry discloses a microprocessor 100 having a fetcher 101 that fetches instructions according to the contents of an instruction pointer (IP) 142. The microprocessor 100 also includes a branch predictor 103 that controls the selection of the contents to be loaded into the IP 142 based upon a prediction of whether a conditional branch instruction will be taken. (*See* column 6, line 53 to column 7, line 16.) The branch instruction address is piped downed with the branch instruction through the various stages of the microprocessor pipeline via registers. (*See* column 7, lines 28-31.) The branch predictor 103 also indicates information relating to its static prediction of the outcome of a conditional branch. The static prediction information is stored in a static prediction register and is piped down with the conditional branch instruction through the various stages of the pipeline via static predictor registers. (*See* column 7, lines 44-53.)

Regarding Claim 22, which is now substantially incorporated into Claim 1, the Examiner states:

> Henry has taught the mechanism as recited in claim 1, wherein said link pointers move through each register set as at least one instruction move through each of said corresponding stages (column 7, lines 25-45, In Figure 1 of Henry, the pointers move through elements 134, 144, 136, 146, 138, 148, 130, and 140 as the instructions move

through each of the Register, Address Data and Write back stages. (Examiner's Action, page 6).

Column 7, lines 25-45 of Henry states:

> The branch predictor 103 receives the address of branch instructions from the IP 142 via signal 188 and uses the branch address to index into a history table storing Agree/Disagree predictions, described below. The branch instruction address is piped down with the branch instruction through the various stages of the pipeline via registers 144, 146, 148 and 140. The branch predictor 103 receives the branch instruction address, which was piped down along with the branch instruction, via signal 186, and uses the branch instruction address to update the Agree/Disagree history table. The branch predictor 103 makes conditional branch instruction outcome predictions based upon a static branch prediction based upon the test type of the conditional branch instruction specifying a condition upon which the conditional branch instruction will be taken, upon an opcode of an instruction preceding the conditional branch instruction and upon a sign of a displacement for calculating a target address of the conditional branch instruction...

Acquiescing *arguendo,* to the characterizations made by the Examiner of Henry regarding Henry reading upon Claim 22, Henry still does not disclose or suggest a mechanism for identifying and tracking conditional instructions as claimed in amended Claim 1. In amended Claim 1, which incorporates language from previously dependent Claim 22, link pointers are moved *through each register of a register set* as an instruction moves through each corresponding stage of a plurality of stages... *wherein the corresponding stages further comprise: a fetch/ decode stage and a group stage.* (Emphasis added).

Furthermore, as claimed in dependent Claim 24, *the fetch/ decode stage is configured to: fetch and decode instructions and identify conditional execution instructions and generate link pointers* [wherein the link pointers mark at least the beginning and end of a conditional execution block of instructions, as described in amended Claim 1]. In dependent Claim 24, the group stage is

configured to *check grouping and dependency rules, group valid instructions, execute return instructions; and group conditional execution instructions and blocks.* (Emphasis added)

Henry does not teach or suggest stages as claimed in amended independent Claim 1, nor as further defined and claimed in dependent Claim 24. In Henry, although, *arguendo*, pointers may move through elements 134, 144, 136, 146, 138, 148, 130, and 140 as instructions move through each of the so-called "Register, Address Data and Write back stages" (Examiner's Action, page 6), Henry does not disclose or suggest pointers moving through a "fetch/ decode stage" and a "group stage" as defined in presently claimed in amended Claim 1, nor as claimed and defined in dependent Claim 24.

Nor does Park compensate for the deficiencies of Henry. Park relates to a branch prediction method using an address trace. In Park, an address trace corresponding to an executed instruction is stored itself with a decoded form. After appointing a start address and an end address of a repeated routine, current routine iteration count and total number of iterations are compared with each other, purportedly confirming the end of the routine and storing address information of the next routine. (Abstract).

Additionally, the Examiner does not cite Park for a disclosure or a teaching of link pointers that move through each register of each register set as at least one instruction move through each of a corresponding stage. Furthermore, Applicants respectfully state that Park does not disclose or suggest *wherein the stages further comprise: a fetch/ decode stage and a group stage* as claimed in amended independent Claim 1 and further defined in dependent Claim 24. (Emphasis added).

Therefore, Henry, individually or in combination with Park, fails to teach or suggest the invention recited in independent Claims 1 and its dependent claim, when considered as a whole. For analogous reasons, Henry, individually or in combination with Park, also fails to teach or suggest the invention recited in independent Claims 8 and 15 and their dependent claims, when considered as a whole. Claims 1-4, 6-11, 13-18, 20-21, 24-26 are therefore not obvious in view of Henry and Park.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 1-4, 6-11, 13-18, 20-21 and 24-26 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-4, 6-11, 13-18, 20-21 and 24-26.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present Application. The Applicants reserve the right to disagree with arguments and characterizations made in the present Examiner's Action in a future Response or Amendment.

The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 12-2252.

Respectfully submitted,

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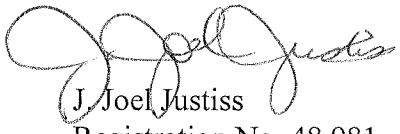

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